REMARKS

Reconsideration of the application is requested.

With regard to the telephone interview that was held with the Examiner on August 27, 2007, counsel affirms the substance of the Interview Summary provided by the Examiner. The Examiner agreed that the Office Action mailed on August 8, 2007 should have been non-final and agreed to send out a new non-final Office Action.

The Examiner mailed out a superceding non-final Office Action on August 29, 2007 and reset the time to reply to start from that date. Counsel appreciates the courtesy and prompt action taken by the Examiner.

Claims 1-9 remain in the application. Claims 1-9 are subject to examination. Claims 1-9 have been amended.

Under the heading "Claim Rejections – 35 USC § 101" on page 2 of the above-identified Office Action, claims 1-9 have been rejected as being directed towards non-statutory subject matter under 35 U.S.C. § 101.

Applicant does not agree that a configuration is non-statutory, however, in the interest of advancing prosecution, applicant has directed all of the claims to a circuit. Applicant believes it is clear that a program controller is a circuit and that a circuit is statutory subject matter.

Additionally, claims 2, 4, 5, 6, and 9 have been amended to delete the term "configured for". Support for the changes to those claims is inherent in the claims as originally presented. Claim 8 has also been amended to delete the term "configured for". Support for the change to claim 8 may be found by referring to the specification at page 11, lines 4-8.

With regard to the Examiners comments in items 5 and 6 on page 3 alleging that there is no useful, tangible, and concrete result, applicants respectfully disagree. Applicant teaches that it is important to be able to test whether pipeline stages are stopped correctly (page 5, lines 5-8; and page 10, line 19 through page 11, line 2). Applicant teaches that by enabling the program controlled unit to execute instructions that instruct it to stop specific pipeline stages, particular conditions do not have to be created for stopping particular pipeline stages (page 6, lines 20-25; and page 10, lines 8-14). Applicant also teaches that in order to stop specific pipeline stages, without using the present invention, the conditions that would be needed would be difficult to create (page 5, lines 10-13).

Additionally, the Examiner has cited two references, which the Examiner alleges are related to stopping or delaying pipeline stages.

Applicant believes it has been clearly shown that providing a program controlled unit for executing pipeline instructions in order to stop specific

pipeline stages does, in fact, produce a result that is useful, tangible, and concrete.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 101. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

Under the heading "Claim Rejections – 35 USC § 103" on pages 3-5 of the above-identified Office Action, claims 1-9 have been rejected as being obvious over U.S. Patent No. 6,163,837 to Chan et al. in view of U.S. Patent No. 6,609,193 B1 to Douglas et al. under 35 U.S.C. § 103. Applicant respectfully traverses.

The Examiner has alleged that Douglas et al. teach instructions for stalling pipeline stages. The Examiner has also alleged that one of ordinary skill in the art considering Douglas et al. and Chen would somehow modify Chen to selectively stop particular pipeline stages or "pipestages".

Chen is concerned with stalls that occur when multiple execution units share a write port (column 1, lines 24-37). Chen merely teaches that when there is a long latency instruction, either the compiler or the programmer can insert a

NOP instruction so that a bubble will occur in the A3 stage that delays the trap stage T (column 7, lines 44-55).

The teaching in Douglas et al., however, does not relate to a software instruction, such as a NOP, but rather relates to the evaluation of hardware signals dependent upon the operational condition of certain pipestages at particular times. In particular, control algorithm equations are implemented in hardware by the control logic 401 to control whether the clock signal is applied to the pipestage (See column 8, line 55- column 9, line 36 and Fig. 4). The output of the control algorithm equations are dependent upon hardware signals obtained, for example from the instruction valid bits of the pipestages, the instruction thread ID of the instruction in a pipestage, and the multiplexer outputs 606A-606M.

Just how would one modify a NOP software instruction in view of a teaching about controlling the clock of a pipestage based on hardware signals indicating certain operational conditions of a pipestage? Applicant respectfully believes that one of ordinary skill in the art considering the hardware stall signal in Douglas et al. would certainly not arrive at an obvious modification to a NOP instruction. If the Examiner disagrees, applicant respectfully requests that the Examiner explain his point of view as to just how such a modification would be performed.

Additionally, the Examiner has alleged that Fig. 7 of Douglas et al. shows instructions for stalling. Fig. 7 shows control algorithm equations executed by the control logic 401 (See column 8, lines 55-57 and Fig. 4). These equations, which are executed by the control logic 401, are not pipeline instructions as specified by claim 1.

Claim 1 specifies:

> said program-controlled unit executing pipeline instructions instructing said program-controlled unit to stop an individual one of said plurality of pipeline stages, more than one of said plurality of pipeline stages, or all of said plurality of pipeline stages without creating any conditions for which one pipeline stage, a plurality pipeline stages, or all pipeline stages are stopped.

To further emphasize the point that the control algorithm equations are not pipeline instructions that are executed, applicant will discuss the teaching of Douglas et al. related to the control algorithm equations in detail. Fig. 4 shows that the pipeline instructions 410 are input to and are processed by the instruction decode pipeline 400. Fig. 4 also shows the control logic 401 that implements the control algorithm equations. The control logic 401 consists of common hardware logic elements connected to implement the control algorithm equations in the manner described at column 8, line 57 - column 9, line 36. The control logic 401 includes powerdown logic 603 that operates by ANDing instruction valid bits as described at column 9, lines 1-13 in accordance with

the equations shown in Fig. 7. The control logic 401 also includes clear logic 605A – 605M, which is described at column 9, lines 14-36, and which operates in accordance with the equation labeled $Clear_{(X)}$ shown in Fig. 7.

Additionally, Douglas et al. teach that a stall signal is generated by the buffers 502A, 502B to stall the instruction decode pipeline 400' when a respective buffer 502A, 502B becomes full and cannot accept additional instructions (See column 6, lines 63-67; see also column 7, line 54 through column 8, line 4).

It should be clear that the control algorithm equations, which are implemented by the control logic 401, are not pipeline instructions that are executed as specified by claim 1. Therefore, even if the teachings in Chan and Douglas et al. were combined in some manner for some reason, the claimed invention could not have been obtained.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited.

Applicant reminds the Examiner that claims 1-9 have been amended solely to address the 35 USC § 101 rejection.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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MPW:cgm

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